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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,919	07/31/2001	Junichi Yoshizawa	04329.2618	2102

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EXAMINER	
SHAH, CHIRAG G	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,919	YOSHIZAWA, JUNICHI	
	Examiner	Art Unit	
	Chirag G. Shah	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,9,11 and 27* is/are rejected.

7)☒ Claim(s) *2-5,7,8,10 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The elected claims 1-14 and 27 has examined on the merit.

Claim Objections

1. Claims 3, 8, 13, and 14 are objected to because the respective claims recite the limitation "capable of". Under MPEP 2106, page 2100-8, "language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation." Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 9 rejected under 35 U.S.C. 102(b) as being anticipated by Ando et al. (U.S. Patent No. 5,625,847), hereinafter Ando.

Regarding claim 9, Ando discloses an information processing apparatus [see fig. 1, controller 12] comprising:

a system bus [BUS 21, fig. 1];

a CPU connected to the system bus [CPU 11, fig. 1];

a memory connected to the system bus [system memory 13 connected to bus 11, see fig. 1];

a data transmission/reception unit transmitting and receiving data to and from a network [CPU interface 121 for transmitting and receiving data, see fig. 1];

a first external input/output interface controller [PCMCIA controller 14, fig. 1] controlling a first external input/output interface with an external unit [PCMCIA controller 14 inherently controls various PC cards];

a second external input/output interface controller [IDE 15 or SCSI 16 or other I/O controllers 17, see fig. 1] controlling a second external input/output interface with the external unit [Each of the respective controllers respectively inherently controls its PC card]; and

an input/output switching unit [Selector 126, fig. 1] selectively forming a data path among the first external input/output interface [PCMCIA Controller 14, fig. 1], the second external input/output interface [IDE 15 or SCSI 16 or other I/O controllers 17, see fig. 1], the system bus [Bus 21, fig. 1] and the data transmission /reception unit [CPU interface 121, fig. 1].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, 11 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Ando et al. (U.S. Patent No. 5,625,847), hereinafter Ando in view of Zenda (U.S. Patent No. 5907,686).

Regarding claims 1 and 27, Ando discloses an information processing apparatus [see fig. 1, controller 12] comprising:

a system bus [BUS 21, fig. 1];

a CPU connected to the system bus [CPU 11, fig. 1];

a memory connected to the system bus [system memory 13 connected to bus 11, see fig. 1];

a data transmission/reception unit transmitting and receiving data to and from a network [CPU interface 121 for transmitting and receiving data, see fig. 1];

an external input/output interface controller controlling an input/output interface with an external unit [PCMCIA Controller 14, fig. 1 and col. 5, lines 10-25]; and

an input/output switching unit [selector 126, fig. 1 and col. 6, lines 10-25] selectively forming a data path among the data transmission/reception unit [CPU interface 121, fig. 1] and the external input/output interface controller [PCMCIA Controller 14, fig. 1].

Ando fails to disclose of an encoding/decoding unit encoding and decoding data and forming a data path from the input/output switching unit and the encoding/decoding unit. Zenda discloses in fig. 1 and in col. 4, lines 1-20 of MPEG sound decoder 24 and MPEG video decoder 25 for decoding the encoding signal. The sound and video controllers are controlled by the PCMCIA controller 16 as disclosed in figure 1. Thus, clearly establishing a data path from the switching unit and decoding unit. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Ando to include the teachings of voice and video decoders under the control of the PCMCIA controller in order to

expand the compressed sound and image data stored in the memory ensuring the output of a high-quality image and sound data.

Regarding claim 6, Ando discloses an information processing apparatus [see fig. 1, controller 12] comprising:

a system bus [BUS 21, fig. 1];

a CPU connected to the system bus [CPU 11, fig. 1];

a memory connected to the system bus [system memory 13 connected to bus 11, see fig. 1];

a data transmission/reception unit transmitting and receiving data to and from a network [CPU interface 121 for transmitting and receiving data, see fig. 1];

an external input/output interface controller controlling an input/output interface with an external unit [PCMCIA Controller 14, fig. 1 and col. 5, lines 10-25];

an input/output switching unit [selector 126, fig. 1 and col. 6, lines 10-25] electively forming a data path among external input/output interface controller [PCMCIA Controller 14, fig. 1], said system bus [BUS 21, fig. 1], said data transmission/reception unit [CPU interface 121, fig. 1] and

Ando fails to disclose of an encoding/decoding unit encoding and decoding data and forming a data path from the input/output switching unit and the encoding/decoding unit. Zenda discloses in fig. 1 and in col. 4, lines 1-20 of MPEG sound decoder 24 and MPEG video decoder 25 for decoding the encoding signal. The sound and video controllers are controlled by the PCMCIA controller 16 as disclosed in figure 1. Thus, clearly establishing a data path from the

switching unit and decoding unit. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Ando to include the teachings of voice and video decoders under the control of the PCMCIA controller in order to expand the compressed sound and image data stored in the memory ensuring the output of a high-quality image and sound data.

Regarding claim 11, Ando discloses an information processing apparatus [see fig. 1, controller 12] comprising:

a system bus [BUS 21, fig. 1];

a CPU connected to the system bus [CPU 11, fig. 1];

a memory connected to the system bus [system memory 13 connected to bus 11, see fig. 1];

a data transmission/reception unit transmitting and receiving data to and from a network [CPU interface 121 for transmitting and receiving data, see fig. 1];

an external input/output interface controller controlling a second external input/output interface with the external unit [PCMCIA Controller 14, fig. 1 and col. 5, lines 10-25];

an input/output switching unit [selector 126, fig. 1 and col. 6, lines 10-25] selectively forming a data path among the data transmission/reception unit [CPU interface 121, fig. 1] and the external input/output interface controller [PCMCIA Controller 14, fig. 1].

Ando fails to disclose of a voice and image encoding/decoding unit encoding and decoding voice data and a voice/image multiplexing/demultiplexing unit conducting voice and image multiplexing and demultiplexing to the voice data and the image data; Ando also fails to

disclose of forming a path among the data transmission reception unit, voice encoding/decoding unit, and voice/image multiplexing unit. Zenda discloses in fig. 1 of voice 15 card video mux 17c for multiplexing voice and video data respectively. Zenda discloses in fig. 1 and in col. 4, lines 1-20 of MPEG sound decoder 24 and MPEG video decoder 25 for decoding the encoding signal. The sound and video controllers are controlled by the PCMCIA controller 16 as disclosed in figure 1. Thus, clearly establishing a data path from the switching unit and decoding unit and multiplexing unit. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Ando to include the teachings of voice and video decoders under the control of the PCMCIA controller in order to expand the compressed sound and image data stored in the memory ensuring the output of a high-quality image and sound data.

Allowable Subject Matter

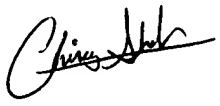
6. Claim 3, 4-5, 7, 10, and 12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
December 22, 2005



Chirag Shah
Patent Examiner, AU 2664